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FUNCTIONAL DESCRIPTION OF THE DREO LTN-51 ARINC BUS/LSLI-11 DRV--ETC(U)
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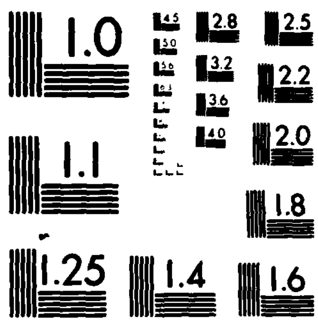

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FUNCTIONAL DESCRIPTION OF THE DREO LTN-51 ARINC BUS/LSI-11 DRVII-C INTERFACE,

by

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Electromagnetics Section
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ABSTRACT

An interface between the ARINC bus of a Litton LTN-51 navigation system and an LSI-11 minicomputer was designed and built for use in recording flight data on board a Convair 580 flight research aircraft.

The interface accepts serial, binary data from the LTN-51 and transfers this data to the LSI-11 through a Digital Equipment Corporation standard DRV11-C parallel interface.

RÉSUMÉ

Une interface entre le bus ARINC d'un système de navigation Litton LTN-51 et un mini-ordinateur LSI-11, a été conçue et assemblié pour utilisation lors d'enregistrements de données de vol à bord d'un avion de recherche Convair 580.

L'interface accepte des données binaires en série du LTN-51 et transfert ces données au LSI-11 au moyen d'une interface standard (parallèle) de DEC, le DRV11-C.

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1.0 BACKGROUND

An interface was designed and constructed at the Defence Research Establishment Ottawa (DREO) to receive serial binary data from the ARINC bus of the Litton LTN-51 inertial navigation system. In addition, it was required to transfer the data to an LSI-11 minicomputer through a standard Digital Equipment Corporation (DEC) DRV11-C 16-bit parallel interface for airborne recording purposes. Flight records were to be obtained using the NAE Convair 580 aircraft when testing various inertial navigation systems. The LTN-51 was used as the reference navigator for testing other systems and to support research and development work at DREO in the field of navigation. This Technical Note summarizes the operation of both the LTN-51 ARINC bus, the DRV11-C interface in the LSI-11 minicomputer, and describes the operation of the interface designed to operate between the two systems.

Because it was necessary to develop the interface quickly (to conform to Convair flight schedules) the hardware employed was not optimized in terms of space and power consumption. The components however, are inexpensive and are readily available.

2.0 LTN-51 ARINC BUS

The purpose of the interface is to collect data words from the Litton LTN-51 navigation system ARINC bus and record this data on magnetic tape through an LSI-11 minicomputer. The data from the LTN-51 is available on the ARINC bus in serial, binary format. The ARINC bus provides three, twisted-pair output lines; the data line, the synchronization line, and the clock line. The data rate is 13.8 KHz. The relationship between these lines is shown in Figure 1. Each data word from the LTN-51 is 32 bits long and is transmitted with the Most Significant Bit (MSB) first. The 8 MSB's comprise the address, the remaining 24 bits contain the data word. The synchronization line is used to signal the beginning of each 32-bit word as well as the end of the address bits (see Figure 1).

The binary data words available from the ARINC bus are listed in Figure 2. For the purposes of this interface, only 6 of these data words were desired:

- Present Position Latitude
- Present Position Longitude
- Ground Speed
- Track Angle
- North-South Velocity
- East-West Velocity

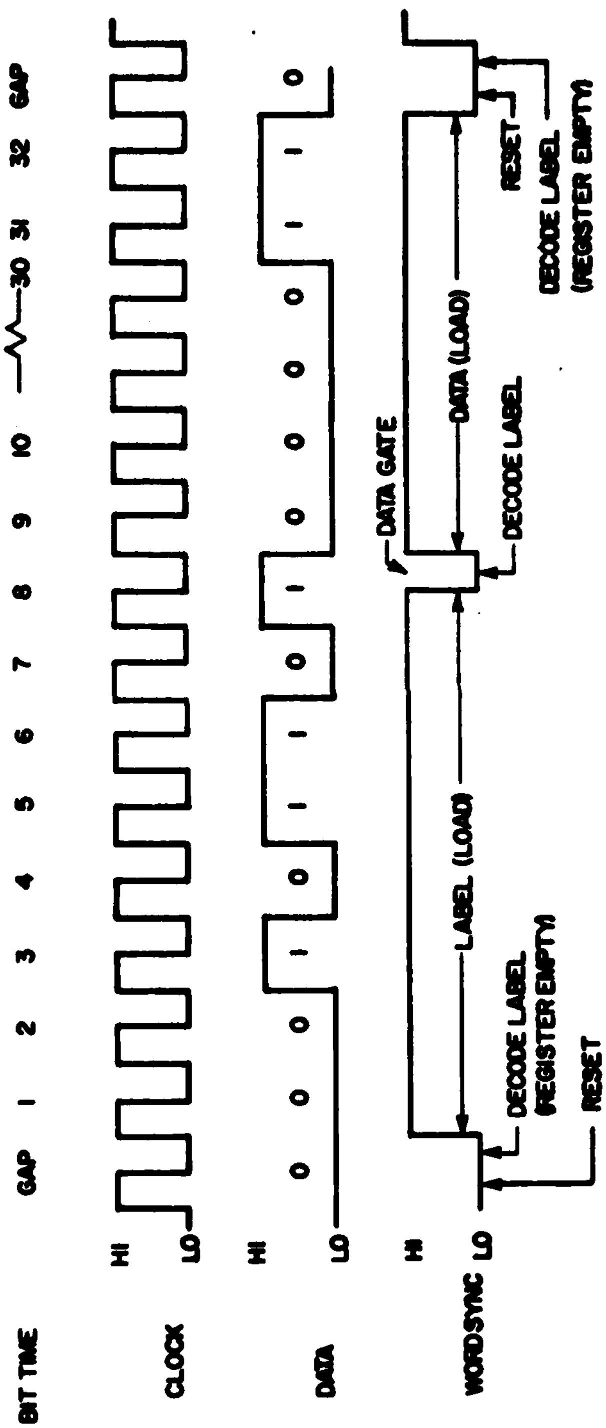


Figure 1. ARINC 6 - Wire Timing Diagram

Parameter	Qty	Range	Units	Resolution	Sig* Bits	Note
Present Position latitude	1	0 to $\pm\ \pi/2$	Radians	$2\pi/2^{18}$	17	Resolution is approx 5.0 arc-sec
Present-Position longitude	1	0 to $\pm\ \pi$	Radians	$2\pi/^{18}$	17	Resolution is approx 5.0 arc-sec
Ground Speed	1	±3276.7K	Knots	0.1 Knot	15	**
Actual track angle	1	0 to 2π	Radians	$2\pi/2^{13}$	12	Resolution is approx 2.64 arc-min
True heading	1	0 to 2π	Radians	$2\pi/2^{13}$	12	Resolution is approx 2.64 arc-min
Wind speed	1	±3276.7K	Knots	0.1 Knot	15	**
Wind speed	1	$\pm\pi$	Radians	$2\pi/2^{13}$	12	Resolution is approx 2.64 arc-min
N/S velocity	1	±3276.7K	Knots	0.1 Knot	15	
E/W velocity	1	±3276.7K	Knots	0.1 Knot	15	**
Waypoint latitude	9	$\pm\pi/2$	Radians	$2\pi/2^{18}$ R	17	Resolution is approx 5.0 arc-sec
Waypoint longitude	9	$\pm\pi$	Radians	$2\pi/2^{18}$ R	17	Resolution is approx 5.0 arc-sec

Figure 2. LTN-51 Output-Binary Data

* *Number of significant bits does not include sign*

* *Max range of two's complement data format - not system capability*

3.0 LSI-11 DRV11-C INTERFACE

The DRV11-C is a 16-bit parallel interface contained within the LSI-11 minicomputer. It consists of 3 registers; a Status and Control Registers (DRCSR), an Output Buffer (DROUTBUF) and an Input Buffer (DRINBUF).

Interrupts from an external source are available on two lines called REQUEST A and REQUEST B and are serviced through vector addresses 300 and 304 respectively. Functioning of the DRV11-C is accomplished through software-controlled status bits in the Control and Status Register including INT ENB A (Bit 06) and INT ENB B (Bit 05) which allow enabling and disabling of the two interrupt requests and CSR0 (Bit 0) and CSR1 (Bit 01) which act as signal lines (flags) to external hardware. The three DRV11-C registers will now be described.

3.1 DRINBUF

DRINBUF is a read-only, 16-bit register which receives input data from external hardware. A 400 nsec. 'DATA TRANSMITTED' pulse is provided to the user while reading is taking place. The end of this pulse signals that the data has been read into the computer.

3.2 DROUTBUF

DROUTBUF is a 16-bit read/write register that is computer loaded and through which data can be transferred to a user's external hardware. A 400 nsec 'NEW DATA READY' pulse signals that data is ready to be transmitted. The trailing edge of this pulse signifies that the data has settled on the user's input lines.

3.3 DRCSR

DRCSR is a 16-bit status register consisting of:

- Bit 15 - REQUEST B
- Bit 07 - REQUEST A
- Bit 06 - INT ENB B
- Bit 05 - INT ENB A
- Bit 01 - CSR1 } user-defined
- Bit 00 - CSR0 } flags

4.0 INTERFACE DESCRIPTION

For the purposes of this interface, only 6 data words were required from the LTN-51. It was desirable to design the interface such that all six of the data words would be selected, read and stored within the interface before being transferred to the LSI-11 through the DRV11-C. This was necessary to reduce the workload on the computer since, in the desired application, several other functions were being performed by the LSI-11.

4.1 WORD STRUCTURE AND SYNCHRONIZATION

Data from the LTN-51 is received on the ARINC bus at 13.8KHz. The timing is such that the binary data words are sent in 32-bit sequences; (the first eight bits comprise the address).

The ARINC standard provides for a 4-bit minimum gap between words and a total of 11 words are sent.

The output voltage levels on the ARINC bus are 0 to 12 volts.

In order to make the data, synchronization and clock lines TTL compatible, HCPL 2630 optically-coupled gates are used at the front end of the interface. These gates provide good isolation and also help eliminate possible ground loops between the ARINC driver circuitry and the interface.

As shown in Figure 1, the synchronization signal goes to a high logic level at the beginning of each data word then returns to a low level for one bit time after the eighth bit before again going to a high level for the remainder of the word. This 'return to zero' function signals the end of the eight address bits.

For the purposes of the interface, it was decided to read all of the binary data words as they were sent on the ARINC bus. The six desired words were obtained by comparing the incoming address bits with a pre-selected address loaded from the LSI-11 into a digital comparator circuit on the interface. Knowing the order in which the data words appear on the ARINC bus allows the computer to load the successive addresses into the comparators provided the interface signals the computer as each address is matched and the data word stored.

Since the incoming data is in serial form, the interface is designed to store each 32-bit word in serial-to-parallel shift registers. Once all 32 bits of a word are stored, the address bits are compared to the pre-selected address on the comparators and, if the addresses match, the 24-bit data word is stored in parallel-to-parallel shift registers.

The synchronization pulse is used to effect the address comparison once all 32 bits of a word have been received. The intent here was to design a circuit that would use the fact that the synchronization pulse is effectively 32 bits long. By removing the 'return-to-zero' after the eighth bit, the lagging edge of this could then be used to signal the

the completed storage of each data word.

Once the data word is received the comparators are enabled, an address comparison is made and the data word is then permanently stored (a desired address) or rejected. If a received word is not one of the desired words, it remains in the serial-to-parallel shift registers until the next word begins and is then shifted out.

Enough data storage is provided in the interface to store six 24-bit data words. Once all six words have been received, an interrupt is sent to the LSI-11 and the data is transferred to the computer through a series of multiplexers.

4.2 CIRCUIT TIMING

A circuit diagram of the interface is shown in Appendix A. At several points in the interface, timing is critical. The two most important areas are in the timing control of the incoming data on the ARINC bus and the data transfer to the DRV11-C. Each of these control circuits will now be described in detail.

4.2.1 ARINC DATA TIMING

As described in the previous section, 32 bits of a data word are received and stored in a shift register before an address comparison is made in the comparators. This is accomplished by modifying the incoming synchronization pulse and using the lagging edge as a 'decode' pulse to enable the comparators. The circuit performing this function includes an SN7474 flip-flop, SN74160 decode counter and an SN7410 dual 3-input NAND gate. A timing diagram showing the signals at various points in the circuit is shown in Figure 3.

The incoming clock pulse is fed through the decode counter to drive the SN74164 shift registers. The SN7474 acts to remove the 'return to zero' of the incoming synchronization pulse. The net effect is to create a 'DECODE' pulse which is exactly 32 bits long. The lagging edge of this pulse is used to enable the SN74LS85 digital comparator inputs. As a result, address comparisons are performed once an entire word has been received and an immediate storage or rejection of the word can be performed depending on the address comparator output.

4.2.2 DATA TRANSFER

Data transfer to the LSI-11 also requires timing control. Once the six 24-bit data words are stored in parallel-in/parallel-out shift registers,

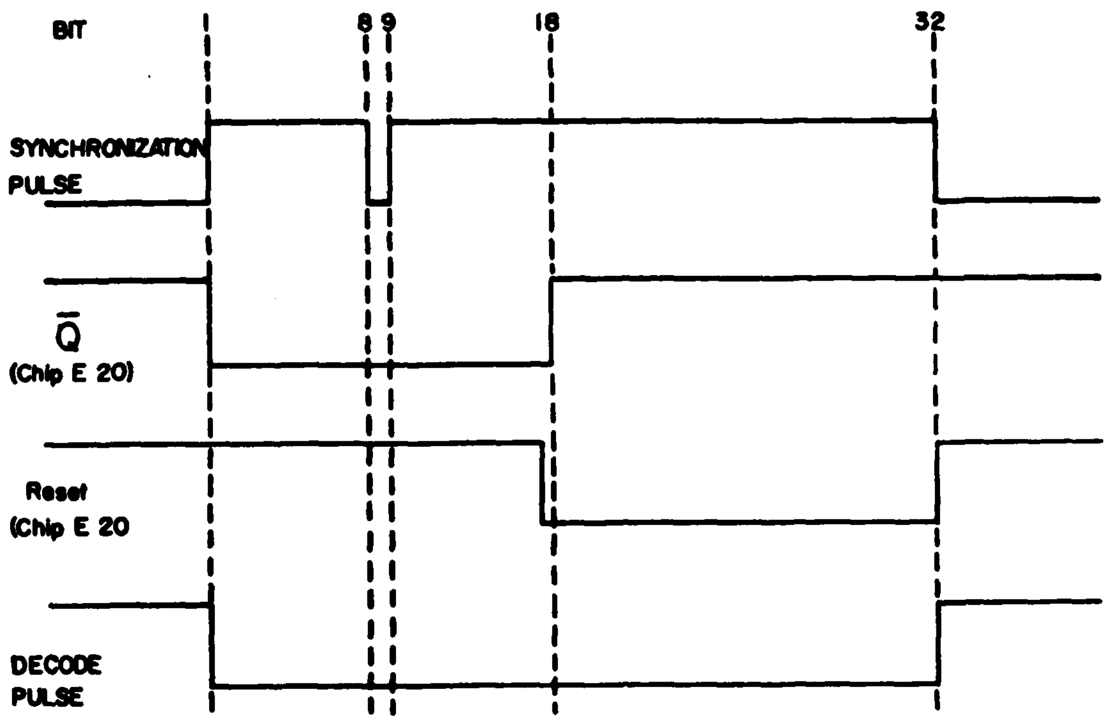


Figure 3. Use of LTN-51 Synchronization Pulse to Provide a 32-Bit Decode Pulse

an interrupt is generated to the DRV11-C REQUEST A line. Since the DRV11-C can only accept 16 bits of parallel data, each data word must be transferred in two parts through a series of SN74LS157 2:1 multiplexers.

It was decided to transfer each 24-bit data word as an 8-bit word (8 MSB's) followed by a 16-bit word (16 LSB's).

As described earlier a 'DATA TRANSMITTED' pulse is provided from the DRV11-C while data is being read. The lagging edge of this pulse signifies that the data has been received by the LSI-11. Using this information, a timing circuit was designed to control the multiplexers and shift registers to read the six data words in the desired sequences. This circuit is shown on the circuit diagram (Appendix A) and consists of an SN74112 flip-flop (lagging edge triggered) and an SN74221 monostable multivibrator. A timing diagram for the data transfer sequence is shown in Figure 4.

The lagging edge of the 'DATA TRANSMITTED' pulse clocks the SN74112 flip-flop controlling the selection of the desired multiplexer channel and this select line in turn triggers the monostable multivibrator to clock the next 24-bit data word into the multiplexers. It should be noted that in order to read the six 24-bit data words, a total of twelve 'DATA TRANSMITTED' pulses (computer reads a data word) are required.

4.3 SOFTWARE CONTROL

The software controlling the interface can best be described by a 'walk-through' of the sequence of events in one cycle of the interface.

The interface is initialized by a RESET pulse from the DRV11-C. This pulse clears the shift registers and cancels all interrupt requests. The first desired address is then loaded into the SN7474 flip-flops on the interface. A list of the relevant addresses is given in Figure 5. Note that although the addresses are 8 bits long, only 6 bits are loaded from the computer. The two Most Significant Bits are always zeroes.

When the synchronization pulse from the LTN-51 begins signifying the start of a data word, the interface accepts all 32 bits of the word, storing them in the SN74164 shift registers. Upon receiving the 32nd bit, the Decode pulse enables a NAND gate resulting in an address comparison in the SN74LS85 digital comparators. If the data address matches the computer-loaded address, the comparators output a pulse which causes the 24 bits of data to be clocked into SN7495 shift registers for storage (a desired word) and this also results in an interrupt to the DRV11-C on the REQUEST B line. Upon receiving this interrupt, the computer loads the next desired address into the comparator circuit flip-flops.

If the desired address and the data address do not match, nothing occurs until the next data word appears and shifts out the undesired word.

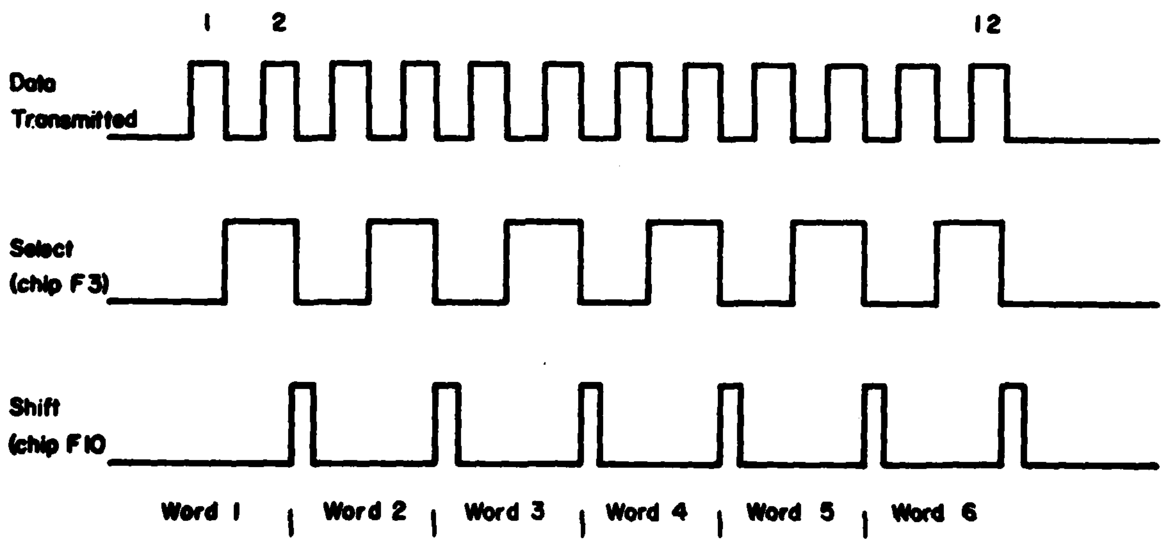


Figure 4. Timing Sequence For Data Transfer to LSI-11

Data Word	Address (MSB)							(LSB)
Present Position Latitude	0	0	0	0	1	0	0	0
Present Position Longitude	0	0	0	0	1	0	0	1
Ground Speed	0	0	0	0	1	0	1	0
Track Angle	0	0	0	0	1	0	1	1
N-S Velocity	0	0	1	1	0	1	1	0
E-W Velocity	0	0	1	1	0	1	1	1
	pre-wired		loaded from DRVII-C					

Figure 5. Binary Data Word Addresses

This sequence carries on until all six data words have been received and stored. As the six words are stored, an SN74197 counter is incremented. Once a count of six is accumulated, the counter generates an interrupt to the DRV11-C REQUEST A line.

At this point, the computer reads the multiplexer output lines twelve times while the interface clocks the appropriate data onto them. When all six data words have been read, the computer reinitializes the interface and the sequence begins again.

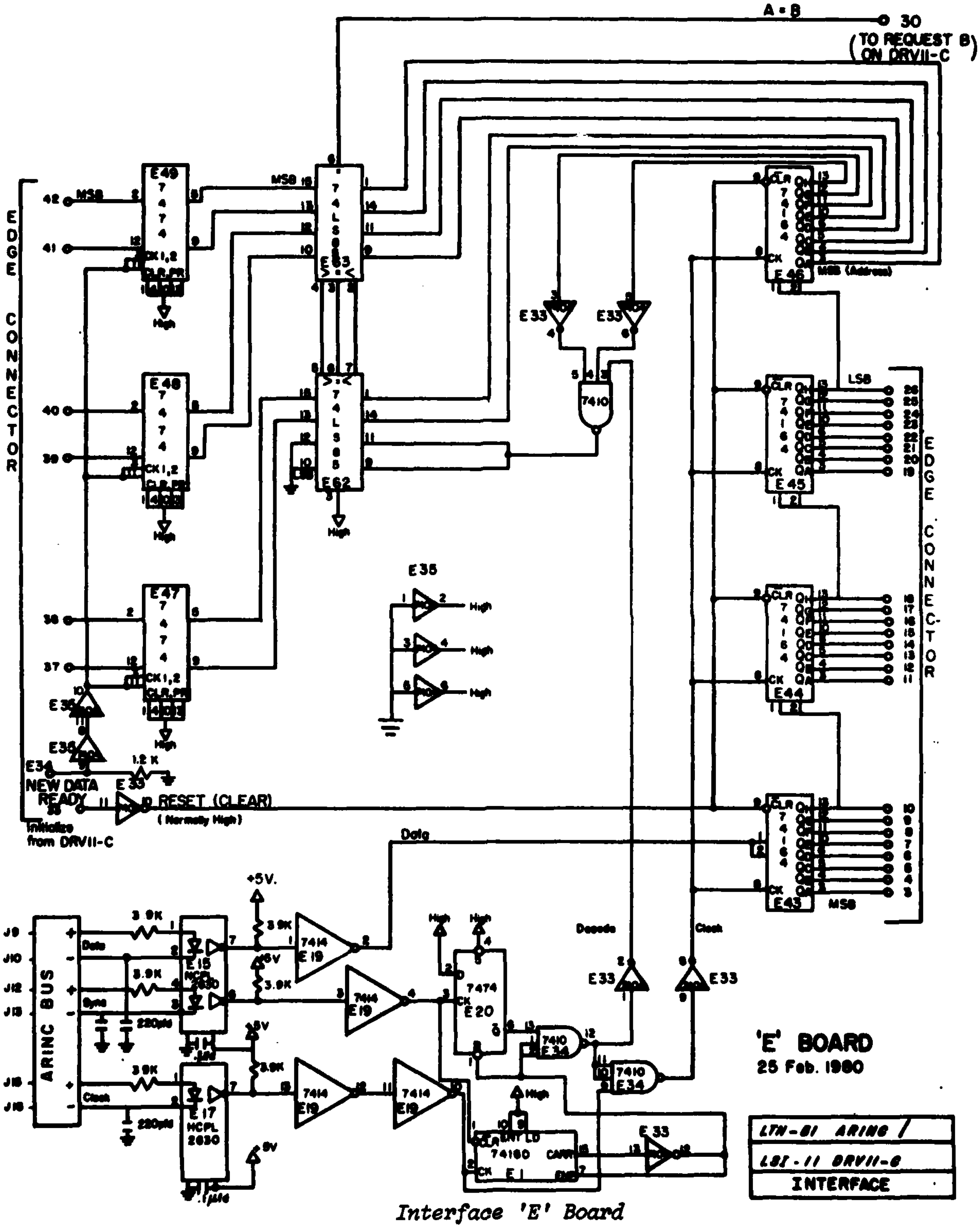
A complete listing of the controlling LSI-11 software is given in Appendix B.

5.0 SUMMARY

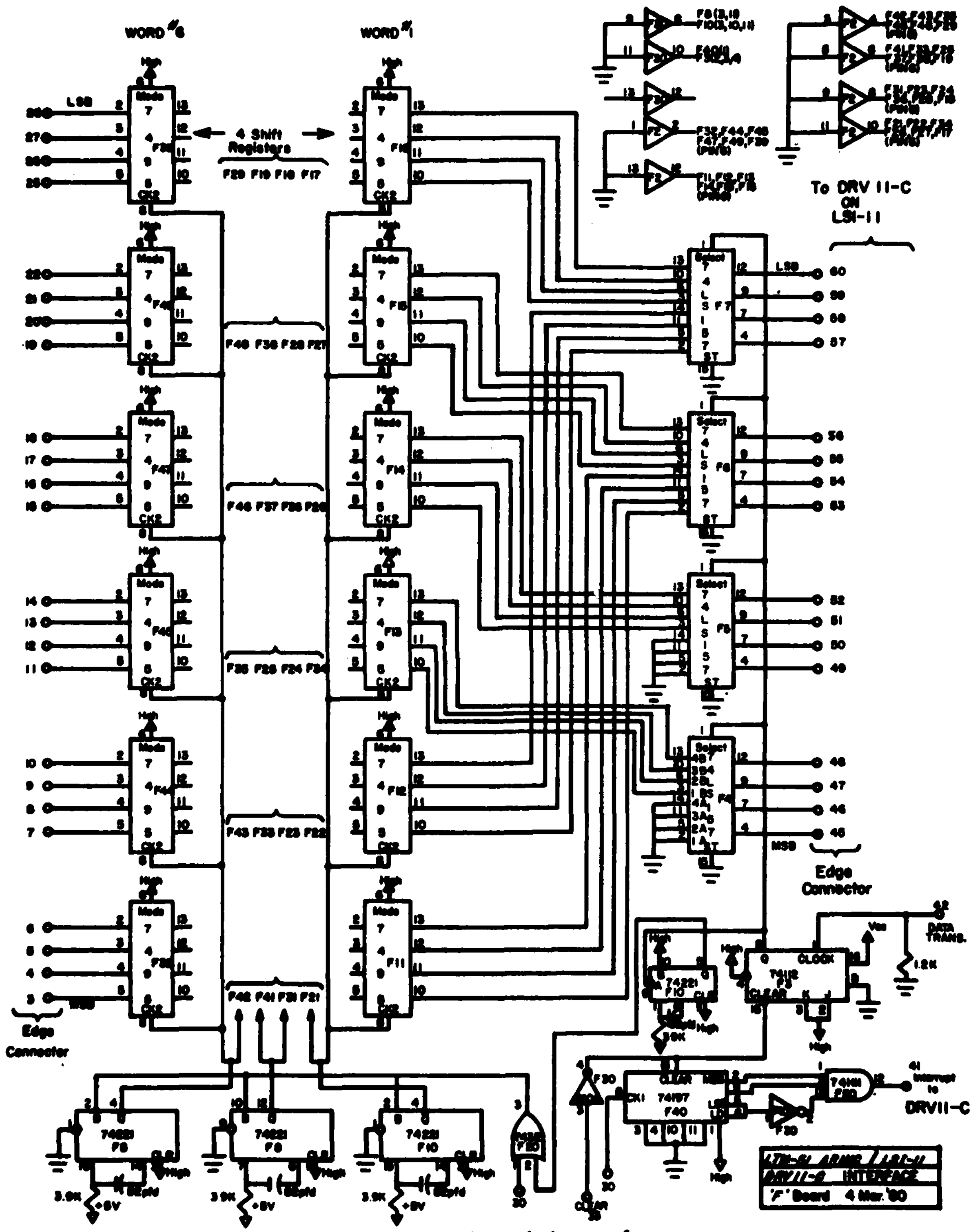
This interface was designed and built at DREO between February and April of 1980. It was installed on board a Convair 580 'flying laboratory' test aircraft in May of 1980 in preparation for summer flight trials and was found to operate as designed.

APPENDIX A

INTERFACE SCHEMATIC DIAGRAM



Interface 'E' Board



Interface 'F' Board

APPENDIX B

INTERFACE SOFTWARE

```
        .TITLE LTN51INTERFACE
LTN51::
        R0=%0
        R1=%1
        R2=%2
        R3=%3
        R4=%4
        R5=%5
        SP=%6
        PC=%7
        MOV #REQA,@#310         ;LOAD ADDRESS OF OUTPUT SERVICE
                                ;INTO INTERRUPT VECTOR
        MOV #340,@#312          ;SET PRIORITY OF OUTPUT SERVICE
        MOV #REQB,@#314         ;LOAD ADDRESS OF INPUT SERVICE INTO
                                ;INTERRUPT VECTOR
        MOV #340,@#316          ;SET PRIORITY OF INPUT SERVICE
        MOV #4,LATAD
        MOV LATAD,@#167762      ;LOAD FIRST ADDRESS (LATITUDE) INTO
                                ;INTERFACE COMPARITOR
        MOV #ADDR,R2            ;LOAD ADDRESSES OF LAST 5 PIECES OF
        MOV #44,(R2)+           ;DATA INTO ARRAY ADDR, 44=LONGITUDE
        MOV #24,(R2)+           ;24=GROUND SPEED,64=TRACK ANGLE,
        MOV #64,(R2)+           ;33=N-S VELOCITY
        MOV #33,(R2)+           ;73=E-W VELOCITY
        MOV #73,(R2)+           ;
        BIC #1,167760           ;START INTERFACE BY TOGGLING BIT 0
        BIS #1,167760           ;OF THE DSCR
        BIC #1,167760
        MOV #6,KNT              ;SET ADDRESS COUNT
        MOV #ADDR,MNT
ENAB:   BIS #140,@#167760       ;ENABLE INTERRUPTS
LOP:    BIT #2,@#167760
        BEQ LOP
        BIC #2
        BR ENAB
REQB:   BIC #100,@#167760       ;DISABLE INTERRUPT B
        DEC KNT                 ;DECREAMENT ADDRESS COUNT
        BNE B1                  ;IF COUNT=0 RELOAD FIRST ADDRESS
        MOV LATAD,@#167762
        MOV #6,KNT              ;RESET ADDRESS COUNT
        MOV #ADDR,MNT           ;
        BIS #100,@#167760       ;ENABLE INTERRUPT B
        RTI
B1:     MOV MNT,R2
        MOV (R2)+,@#167762      ;IF COUNT>0 LOAD NEXT ADDRESS INTO
                                ;INTERFACE COMPARITOR
        INC MNT
        INC MNT
        BIS #100,@#167760       ;ENABLE INTERRUPT B
        RTI
REQA:   BIC #40,@#167760        ;DISABLE INTERRUPT A
        MOV #DATA,R1
        MOV #14,R3
B2:     MOV 167764,(R1)+        ;READ IN 12 WORDS OF DATA
        DEC R3
        BNE B2
        BIS #42,167760          ;ENABLE INTERRUPT A AND SET FLAG
        MOV #ADDR,MNT
        BIC #1,167760           ;CLEAR INTERFACE - TOGGLE BIT 0
        BIS #1,167760           ;OF DSCR
        BIC #1,167760
        RTI
MNT:    .WORD 1
KNT:    .WORD 6
        .PSECT LTNDAT,D,GBL,OVR
DATA:   .BLKW 14
LATAD:  .WORD 0
ADDR:   .BLKW 5
        .END
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13. ABSTRACT

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